FSM based tests' fault coverage for the gate-level circuit design

Evgeny Vinarsky
Moscow State University
Under the framework of the French-Russian Lab QUALIPSO

Paris 2016

Motivation

- Hardware testing is important…

Different abstraction levels:
- FSM / Automata models can be used for this
- Tests can be derived from the logic circuits directly
- …

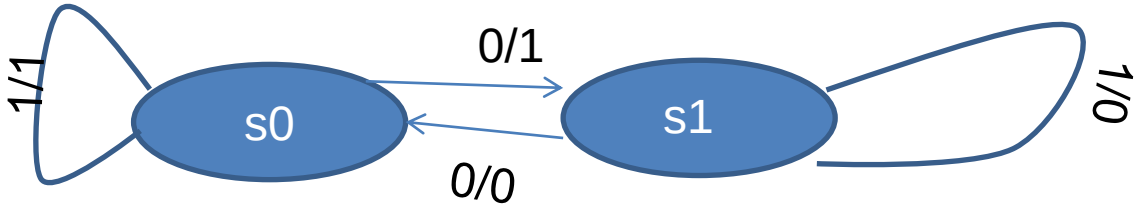
- The question arises: what is the relationship between tests derived for an FSM and a logic circuit which describe the same digital system?

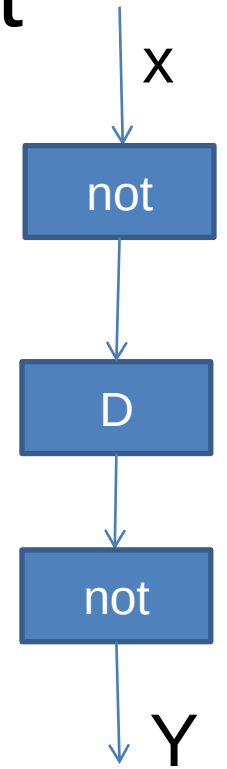
FSM based tests VS logic circuit based tests

FSM tests:	Logic circuit based tests:
Are derived at the high level of abstraction when designing a digital device Have a set of well developed Black Box techniques for the test derivation Detect transition and output faults in the implemented system	Are derived at the low level of abstraction when designing a digital device Have a set of well developed White Box test derivation techniques Usually “take care” of Single Stuck-at Faults, Bridges, etc. that can occur at the logic level

Problem statement : Are FSM tests good enough for detecting faults at the logic circuit level?

Constructing FSM based logic circuit





Given an FSM, in order to derive a corresponding logic circuit, we encode each state, input and output with a Boolean vector

Transition and output FSM functions become Boolean functions and we implement them by the composition of logic gates and latches

Checking FSM tests

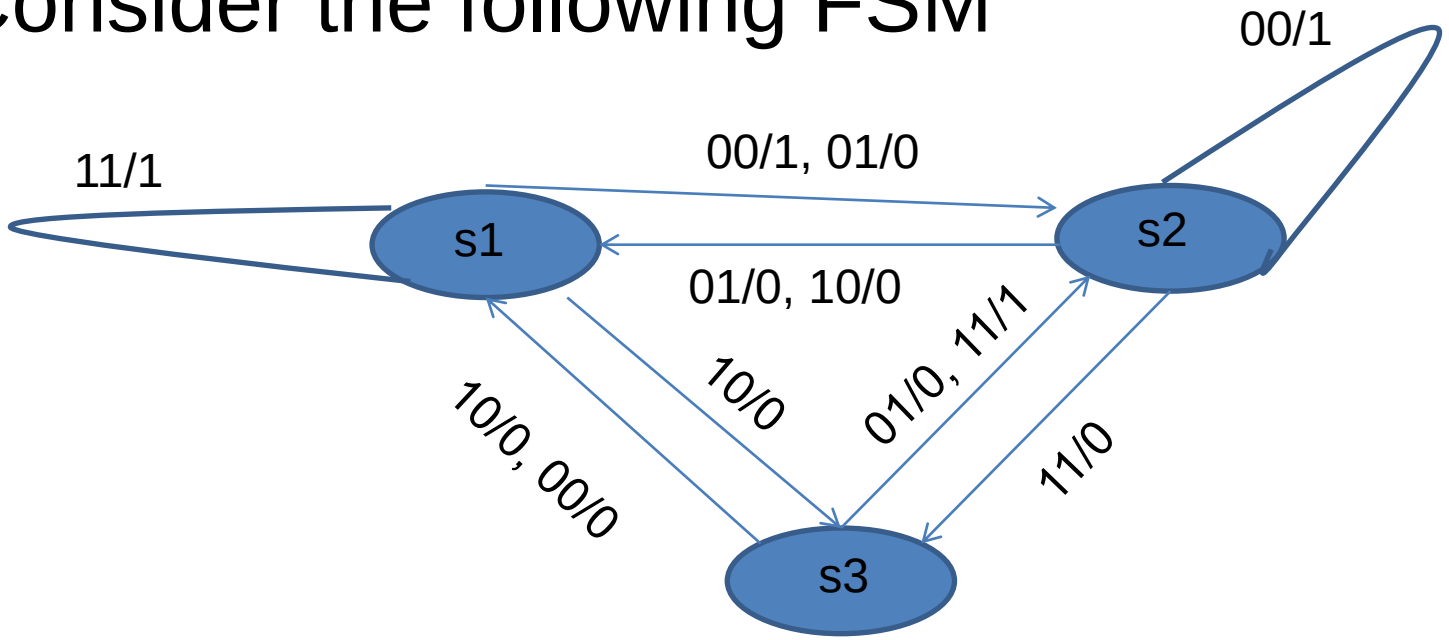
Given an FSM and a corresponding logic circuit
- We derive the transition tour
- And check whether simple logic faults can be detected by the transition tour

For this purpose we…
- Randomly generated FSMs with small number of states and corresponding transition tours
- Derived a corresponding logic circuit
- Randomly replaced a single gate with another gate
- Checked if this fault can be detected by the transition tour

Fast enough we have found an example when a logic fault is not detected

Example

Consider the following FSM



Transition tour for this FSM

11 00 01 01 10 00 11 01 11 11 11 10 10 10

Expected output response is

1 1 0 0 0 1 0 0 0 1 0 0 0 0

What if the circuit is implemented wrongly?

In this mutant, an AND gate is replaced with the XNOR gate

Applying the test sequence, we obtain the expected output response
The fault is not detected ☹
But this bug can be detected by another input sequence

Conclusion: FSM based tests not always detect bugs at the logic circuit level

Conclusions

- FSM based tests do not kill some logic level mutants
- We don’t know if logic level based tests can kill all/some FSM mutants

- Digital device design should address different types of tests at different abstraction levels

Future work :

- To study necessary/sufficient conditions when FSM based tests can guarantee the fault coverage over the logic level circuits
- To perform some experiments to estimate the corresponding fault coverage

Thank you for your attention!

… and for the grant for my participation ☺